UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,148	12/10/2003	Hidetoshi Koike	246360US2S	4814

22850 7590 10/18/2005

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
CHAMBLISS, ALONZO	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/731,148	KOIKE, HIDETOSHI	
	Examiner	Art Unit	
	Alonzo Chambliss	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *9-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/10/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of claims 1-8 in the reply filed on 3/17/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. Claims 9-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 12/10/03 was filed before the mailing date of the non-final rejection on 10/16/05. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

4. The formal drawings filed on 12/10/03 have been approved by the examiner.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4, 7, and 8 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Koike (US 6,392,300).

With respect to Claims 1 and 7, Koike teaches a semiconductor chip 11 (i.e. a substrate serving portion of a chip), an alignment mark 27, 27A, 27B which is formed by part of an uppermost interconnection layer in a multilevel interconnection that is formed on the semiconductor chip 11 and obtained by stacking low-permittivity insulating layers (i.e. BPSG which inherently has a dielectric constant of 3.0 to 2.5) and interconnection layers, the alignment mark 27, 27A, 27B being arranged adjacent to each corner of the semiconductor chip 11, and a conductive member 17, 20, 23, or 26 which is buried in a contact hole formed in the low-permittivity insulating layer below the alignment mark 27, 27A, 27B and contacts the alignment mark 27, 27A, 27B (see col. 5 lines 1-67 and col. 6 lines 1-67; Figs. 10-18).

With respect to Claim 2, Koike teaches wherein the conductive member includes plugs which are buried in contact holes formed in the respective insulating layers in the multilevel interconnection and the alignment mark contacts a surface of the semiconductor chip via the plugs (see Figs. 10-18).

With respect to Claim 3, Koike teaches an element formed in the semiconductor chip and in which the alignment mark is electrically connected to the element (see Figs. 10-18).

With respect to Claim 4, Koike teaches wherein the conductive member is formed by part of an interconnection layer in the multilevel interconnection (see Figs. 10-18).

With respect to Claim 8, Koike teaches wherein the alignment mark has a width of not less than 10 micrometers (see col. 8 lines 20-28).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koike (US 6,392,300) as applied to claim 1 above, and further in view of Ueno (US2005/0140013).

With respect to Claims 5 and 6, Koike fails to disclose a barrier film (i.e. SiCN) which is interposed between a low permittivity insulating layer and an interconnection layer in the multilevel interconnection while preventing oxidization and diffusion of the interconnection layer. However, Ueno discloses a barrier film 106 (i.e. SiCN) which is interposed between a low permittivity insulating layer 101, 104 and an interconnection layer 103 in the multilevel interconnection while preventing oxidization and diffusion of the interconnection layer (see paragraphs 65-68, 71, 75, 85-93; Figs. 1a,1b3b, 3c,4a-4c,5a, 5b, 6a-6c). Thus, Koike and Ueno have substantially the same environment of a

chip with a multilayer dielectric layer with contact plugs. Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate a barrier layer between insulating layer and an interconnection layer in the multilevel interconnection, since the barrier layer would prevent oxidization and diffusion of the interconnection layer as taught by Ueno.

Double Patenting

9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. Claims 1-8 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,392,300. Although the conflicting claims are not identical, they are not patentably distinct from each other because the instant application and the patent both recite an alignment mark with a conductive member in a semiconductor device.

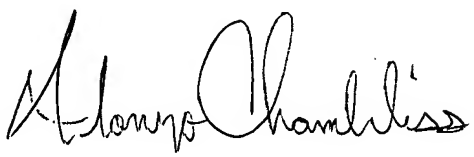
The prior art made of record and not relied upon is cited primarily to show the process of the instant invention.

Conclusion

11. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (571) 272-1927.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system Status information for published applications may be obtained from either Private PMR or Public PMR. Status information for unpublished applications is available through Private PMR only. For more information about the PMR system see http://pair-dkect.uspto.gov. Should you have questions on access to the Private PMR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC_Support@uspto.gov.



Alonzo Chambliss
Primary Patent Examiner
Art Unit 2814

AC/October 16, 2005